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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/057,728	01/25/2002	Clifford Liem	IMP-004 (8326/7)	2788

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EXAMINER	
TO, JENNIFER N	

ART UNIT	PAPER NUMBER
2195	

DATE MAILED: 09/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/057,728	LIEM ET AL.	
	Examiner	Art Unit	
	Jennifer N. To	2195	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 January 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14 and 23-36* is/are pending in the application.

4a) Of the above claim(s) *15-22* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14 and 23-36* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 January 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/28/2002*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-36 are presented for examination.

Election/Restrictions

2. Restriction to one of the following inventions is required under 35 U.S.C. 121:

I. Group I, drawn to claims 1-14, and 23-36 draw to a method of mapping a plurality of tasks and data onto a multiple processor, classified in class 718, subclass 102.

II. Group II, drawn to claims15-22, draw to a method for generating a control graph for a compiler used to map a plurality of tasks and data onto a multiple processor, classified in class 717, subclass 143.

3. Inventions Group I, and Group II are related as subcombinations disclosed as usable together in a single combination. Group I is draw to a method of mapping a plurality of tasks and data onto a multiple processor. Group II is draw to a method for generating a control graph for a compiler. The subcombinations are distinct from each other if they are shown to be separately usable. In the instant case, inventions Group I, and Group II have separate utility such as search for Group I invention is not require for Group II, or Group III invention and vice versa. See MPEP § 806.05(d).

4. Because these inventions are distinct for the reasons given above and have required a separate status in the art shown by their different classification, restriction for examination purposes as indicated is proper.

5. Because these inventions are distinct for the reasons given above and the search required for one group is not required for the other group, restriction for examination purposes as indicated is proper.

6. During a telephone conversation with Mr. Kurt Rauschenbach on 08/23/2005 a provisional election was made with traverse to prosecute the invention of group I, claims 1-14, and 23-36. Applicant in replying to this Office action must make affirmation of this election. Claims 15-22 withdraw from further consideration by the examiner, 37 CFR 1.1142(b), as being draw to a non-elected invention.

7. Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in the application. Any amendment of inventorship must be accompanied by a request under 37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(i).

Claim Rejections - 35 USC § 112

8. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter in which the applicant regards as his invention.

9. Claims 1-14, and 23-36 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

a. The following terms lacks antecedent basis:

i. the multiple processors – claims 1, 4-5, 34, and 36;

ii. the distributed memories – claims 3, 13-14, 34, and 36;

iii. the tasks – claim 6;

iv. the architecture – claims 6, and 35;

v. the least negative – claim 29;

vi. the means for – claim 35;

b. The claim language in the following claims is not clearly understood:

i. as per claim 1, lines 1-2, it is not clearly understood what is meant by "mapping a plurality of tasks and data onto a multiple processor, distributed memory hardware architecture" (i.e. mapping a plurality of tasks and data onto a multiple processor, and mapping a plurality of tasks and data onto a distributed memory). Line 3, it is uncertain what is "a task-level network of behaviors" refers to (i.e. task behaviors). Lines 3-4, it is not clearly understood what is meant by "each of the task-level network of behaviors being related through control and data flow". Lines 6-7, it is not clearly understood how is the step of "allocating the plurality

of tasks and data to at least one of the multiple processors and to at least one of distributed memory, respectively" performed.

ii. as per claim 6, line 2, it is not clearly understood what is meant by "using a resource-based model".

iii. as per claim 9, lines 2, it is not clearly understood what is meant by "using a demand-driven and constraint-base".

iv. as per claim 23, line 5, it is not clearly understood what is meant by "a demand function".

v. as per claim 29, it is uncertain how is the step of "defined as the least negative impact on at least one performance factor" performed (i.e. based on what standard or criteria).

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-14, and 23-36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mattioli et al. (hereafter Mattioli) (WO Patent No. 0060460).

4. As per claim 1, Mattioli teaches the invention substantially as claimed including a method of mapping a plurality of tasks and data onto a multiple processor, distributed memory hardware architecture (page 2, lines 2-5), the method comprising:

a) describing a plurality of operations, each of the plurality of operations being related through control and data flow (page 5, lines12-27; page 6, lines 1-27);

b) predicting a schedule of tasks for the plurality of operations (page 12, lines 5-10); and

c) allocating the plurality of tasks and data to at least one of the multiple processors and to at least one of distributed memory, respectively, in response to the predicted schedule of tasks (page 8, lines 5-27; page 9, lines 1-18).

Mattioli did not specifically teach a task-level network behaviors.

5. However, he disclosed a plurality of operations (page 4, lines 12-15).

6. It would have been obvious to one of an ordinary skill in the art at the time the invention was made to have recognized a plurality of operations is functional equivalent as a task-level network behaviors, representing by high-level language to allow the designer determine the good mapping. Therefore, one would be motivated to utilize this concept for assisting the mapping of systematic signal processing applications onto computer with parallel architecture and allowing at least one optimized mapping solution to be obtained at a level of granularity as fine as possible (page 3, lines 14-17).

7. As per claim 2, Mattioli teaches wherein the predicting the schedule of tasks comprises minimizing execution time of the plurality of tasks (page 20, lines 23-25).

8. As per claim 3, Mattioli teaches wherein the predicting the schedule of tasks comprises minimizing the schedule of tasks by allocating data to the distributed memories in order to minimize data transfers (page 19, lines 11-22).

9. As per claim 4, Mattioli teaches wherein the predicting the schedule of tasks comprises maximizing parallel execution of the plurality of tasks on at least two processors of the multiple processors (page 20, lines 26-27; page 21, line 1).

10. As per claim 5, Mattioli teaches wherein the allocating the plurality of tasks comprises allocating tasks to one of the multiple processors having optimal processor resources for the tasks (page 19, lines 11-22).

11. As per claim 6, Mattioli teaches wherein the predicting the schedule of tasks comprises using a resource-based model of the architecture to predict the schedule of tasks (page 20, lines 7-12).

12. As per claim 7, Mattioli teaches wherein the predicting the schedule of tasks comprises using an interval graph and an execution time model of the task-level

network of behaviors to predict the schedule of tasks (page 7, lines 20-23; page 21, lines 6-10).

13. As per claim 8, Mattioli teaches wherein the allocating the plurality of tasks and data comprises an iterative allocation process (page 5, lines 21-22; page 7, lines 1-19).

14. As per claim 9, Mattioli teaches wherein the iterative allocation process comprises using a demand-driven and constraint-based objective function (page 7, lines 1-19; page 18, lines 6-7).

15. As per claim 10, Mattioli teaches wherein the describing a plurality of operations comprises describing a plurality of operations in a high-level programming language (page 22, lines 26-27; page 23, lines 1-3).

16. As per claim 11, Mattioli teaches wherein the describing the plurality of operations in the high-level programming language comprises parsing the high-level programming language into an intermediate form (page 6, lines 12-14).

17. As per claim 12, Mattioli teaches generating machine executable code for the multiple processors, distributed memory hardware architecture based at least in part on the allocating the plurality of tasks and data (page 18, lines 21-27; page 19, lines 1-22).

18. As per claim 13, Mattioli teaches wherein the allocating the plurality of data to the distributed memories comprises allocating data to shared memories (page 9, lines 11-12).

19. As per claim 14, Mattioli teaches wherein the allocating the plurality of data to the distributed memories comprises allocating data to private memories (page 8, lines 19-21).

20. As per claim 23, Mattioli teaches the invention substantially as claimed including a method for executing a schedule of tasks in a multiple processor, distributed memory architecture, the method comprising:

a) generating the schedule of tasks based at least in part on a plurality of operations (page 5, lines 24-27; page 6, lines 1-4; page 12, lines 5-10);

b) calculating a demand function based at least in part on a constraint related to at least one of a plurality of tasks in the schedule of tasks (page 6, lines 5-8; page 6, lines 20-27; page 8, lines 5-27; page 9, lines 1-18); and

c) allocating a task having highest priority to a processor having least cost according to the demand function (page 10, lines 22-27; page 11, lines 1-27; page 19, lines 6-22).

Mattioli did not specifically teach a task-level network behaviors.

21. However, he disclosed a plurality of operations (page 4, lines 12-15).

22. It would have been obvious to one of an ordinary skill in the art at the time the invention was made to have recognized a plurality of operations is functional equivalent as a task-level network behaviors, representing by high-level language to allow the designer determine the good mapping. Therefore, one would be motivated to utilize this concept for assisting the mapping of systematic signal processing applications onto computer with parallel architecture and allowing at least one optimized mapping solution to be obtained at a level of granularity as fine as possible (page 3, lines 14-17).

23. As per claim 24, Mattioli teaches allocating a data block to a memory in the distributed memory (page 9, lines 11-12).

24. As per claim 25, Mattioli teaches the demand function is calculated based at least in part on the plurality of operations (page 21, lines 2-5).

25. As per claim 26, Mattioli teaches the demand function is calculated based at least in part on an impact on the schedule of tasks (page 12, lines 1-19).

26. As per claim 27, Mattioli teaches the demand function is calculated based at least in part on an impact on data movement (fig. 1; page 12, lines 21-23).

27. As per claim 28, Mattioli teaches the demand function is calculated based at least in part on prior allocation decisions (page 5, lines 2-3).

28. As per claim 29, Mattioli teaches wherein the cost is defined as the least negative impact on at least one performance factor (page 3, lines 3-13).

29. As per claim 30, Mattioli teaches wherein the at least one performance factor comprises the schedule of tasks (page 3, lines 14-19).

30. As per claim 31, Mattioli teaches wherein the at least one performance factor comprises data movement (page 9, lines 3-10, 13-18).

31. As per claim 32, Mattioli teaches a task having next highest priority to a processor having next least cost according to the demand function (page 3, lines 20-27).

32. As per claim 33, Mattioli teaches recalculating the demand function in response to each task in the plurality of tasks being allocated to a processor (page 10, lines 2-9).

33. As per claim 34, it is a system claim that corresponds to method claim 1. Therefore, it is rejected for the same reason as claim 1.

34. As per claim 35, it is rejected for the same reason as claim 11.

35. As per claim 36, Mattioli teaches the multiple processors communicate using the distributed memories (fig. 1).

Conclusion

36. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Spix et al. (U.S. Patent No. 5179702) teaches a system for controlling a highly parallel multiprocessor using an anarchy based scheduler for parallel execution thread scheduling.

Yokoya (U.S. Patent No. 6199093) teaches allocating apparatus employed in multiprocessor system capable of executing a plurality of tasks in a parallel manner, a compiler compiles source program.

Dave (U.S. Patent No. 6415384) teaches hardware/software co-synthesis of dynamically reconfigurable embedded system.

37. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jennifer N. To whose telephone number is (571) 272-7212. The examiner can normally be reached on M-T 7AM- 4:30 PM, F 7AM- 3:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng-Ai An can be reached on (571) 272-3756. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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